VI. Conclusions

We have described a 1 to 2 GHz cooled balanced HEMT amplifier. At a physical temperature of 12 K the amplifier has a noise temperature in the range 3 to 6 K and a gain of ~20 dB. The amplifier was designed primarily as a wide-band IF amplifier for millimeter-wave radio astronomy but it also has applications in wideband L-band receiver systems.

References

[1] S. Weinreb, R. Harris, and M. Rothman, "Millimeter-wave noise parameters of high performance HEMTs at 300 K and 17 K," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1989, pp. 813–816.

[2] K. H. G. Duh *et al.*, "32-GHz cryogenically cooled HEMT low-noise amplifiers," *IEEE Trans. Electron Devices*, vol. 36, pp. 1528–1535, Aug. 1989.

[3] T. H. Buttgenbach *et al.*, "A broad-band low-noise SIS receiver for submillimeter astronomy," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1720–1726, Dec. 1988.

[4] S. Weinreb, "SIS mixer to HEMT amplifier optimum coupling network," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 1067–1069, Nov. 1987.

[5] S. Weinreb, D. Fenstermacher, and R. Harris, "Ultra low-noise 1.2–1.7 GHz cooled GaAs FET amplifiers," NRAO Electronics Division Internal Report No. 220, 1981.

[6] "IRE standards on methods of measuring noise in linear twoports," *Proc. IRE*, vol. 48, pp. 60–68, Jan. 1960.

[7] K. H. G. Duh *et al.*, "Ultra-low-noise cryogenic high electron mobility transistors," *IEEE Trans Electron Devices*, vol. 35, pp. 249–256, Mar. 1988.

[8] J. D. Gallego and M. W. Pospieszalski, "Design and performance of cryogenically-coolable ultra low-noise L-band amplifier," NRAO Electronics Division Internal Report No. 286, 1990.

[9] J. Lange, "Interdigitated stripline quadrature hybrid," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 1150–1151, Dec. 1969.

Equivalent-Circuit Parameter Extraction for Cold GaAs MESFET's

R. Anholt and S. Swirhun

Abstract—**The physical basis of the cold-FET method for extracting parasitic resistances and inductances is examined. A method to obtain the source resistance from the gate-current dependence of the FET Z parameters is used to analyze FET's with different gate lengths. Inductance results for FET's with different gate widths suggest that inductance extrinsic to the gate fingers is dominant, and models of the gate inductance support this. The effects that possible dependences of the parasitic-FET equivalent-circuit parameters on the gate and drain bias can have on the extracted intrinsic-FET parameters are discussed.**

I. Introduction

The cold-FET method provides an elegant way of extracting FET equivalent-circuit parameters (ECP's) from S parameters at any bias [1], [2]. Parasitic source, drain, and gate resistances and inductances are first extracted from measured S parameters of FET's biased at a drain–source voltage $V_{ds} = 0$ and a gate voltage, V_g, greater than the barrier height. With those values fixed, the measured S-parameter matrix for any other bias can be converted to an intrinsic Y-parameter matrix that can be solved exactly for up to eight independent ECP's, depending on the intrinsic-FET circuit topology.

There are two problems with this method. The first is in the cold-FET extraction technique. For the resistances, this can be reduced to a problem of determining two unknowns from only one equation, and we show that this can be solved at forward gate bias. This leads to the second question considered: Is it valid to assume that the cold-FET parameters are independent of bias? If they are not, how much are the extracted intrinsic-FET ECP's (g_m, C_{gs}, etc.) sensitive to possible errors?

In Sections II and III of this paper we examine the problem of extracting the resistances and inductances. Section IV examines the sensitivity of extracted intrinsic-FET ECP's to variations in cold-FET ones.

Manuscript received July 16, 1990; revised March 15, 1991. This work was supported by Honeywell through independent research and development funds.

R. Anholt is with Gateway Modeling, Inc., 1604 East River Terrace, Minneapolis, MN 55414.

S. Swirhun is with the Honeywell Systems and Research Center, Bloomington, MN 55420.

IEEE Log Number 9100154.

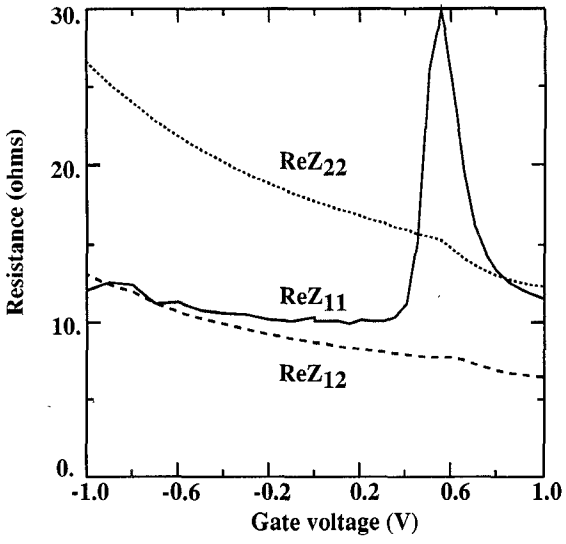

Fig. 1. Real parts of the Z matrices plotted against the gate voltage for an epitaxially doped $1.2 \times 200\ \mu m^2$ MESFET (biased at $V_{ds} = 0$).

II. Source, Drain, and Gate Resistance Extraction

Fig. 1 shows extracted average real parts of Z parameters for FET's biased at $V_{ds} = 0$ plotted against gate potential. With the exception of $\mathrm{Re}\, Z_{11}$ near the peak, when measured S parameters from 1 to 26 GHz are converted to Z parameters, the values are nearly independent of frequency. Two regimes are evident in this figure. For $V_g < 0.6$ V, the Z matrix is given by (parts (c) and (d) of Fig. 2, $g_m = \tau = 0$, $R_{ds} = R_{ch}$, $C_{gs} = C_{gd} = C/2$)

$$
\begin{aligned}
Z_{11} &= R_s + R_{ch}/3 + R_g + j\omega(L_s + L_g) - \frac{1}{j\omega C} \\
Z_{12} &= Z_{21} = R_s + R_{ch}/2 + j\omega L_s \\
Z_{22} &= R_s + R_d + R_{ch} + j\omega(L_s + L_d)
\end{aligned} \tag{1}
$$

where R_s and R_d are the source and drain resistances; R_g is the distributed gate resistance; L_s, L_d, and L_g are the source, drain, and gate inductances; and C is total gate capacitance (including C_{pf} and C_{pg} in Fig. 2(c)). In this regime, the gradual

0018-9480/91/0700-1243$01.00 ©1991 IEEE

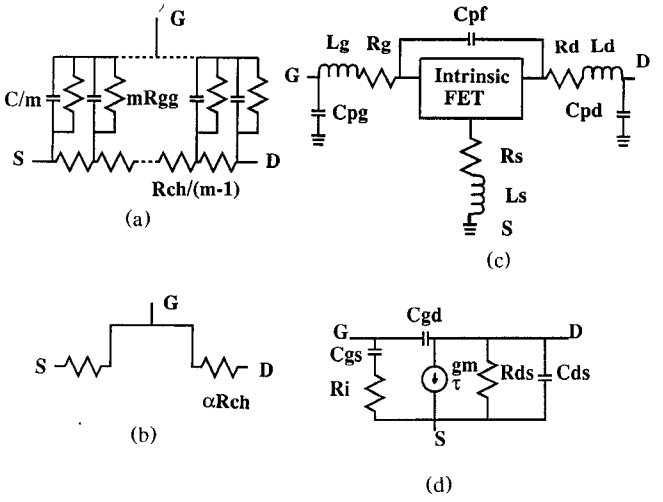

Fig. 2. Various equivalent circuits examined in the text. (a) Distributed gate; (b) large gate current; (c) FET parasitics; (d) intrinsic FET.

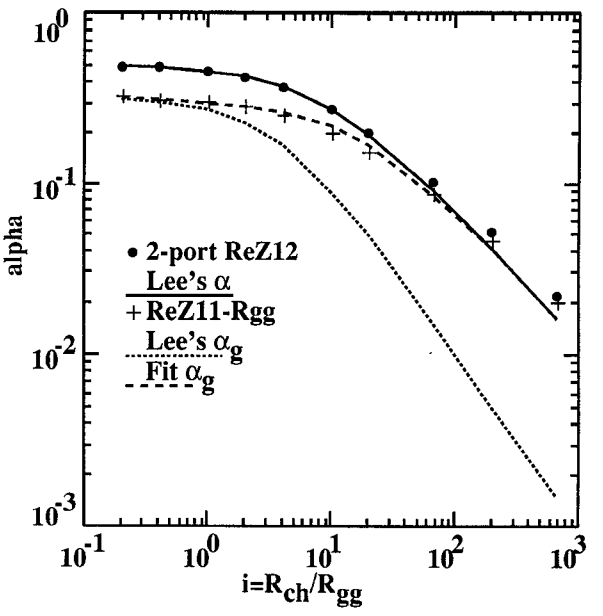

Fig. 3. Calculations of α and α_g from two-port models (R_{12} and R_{11}), Lee's calculations [3] for dc end-resistance measurements, and a fit to our two-port α_g.

falloff in $\mathrm{Re}\,Z_{12}$ and $\mathrm{Re}\,Z_{22}$ is due to the dependence of the channel resistance, R_{ch}, on gate bias.

For $V_g > 0.6$ V, the Z matrix is given by [1]–[4]

$$\begin{aligned} Z_{11} &= R_s + R_{ch}\alpha_g + R_g + R_{gg} + j\omega(L_s + L_g) \\ R_{gg} &= nkT/I_g \\ Z_{12} &= Z_{21} = R_s + \alpha R_{ch} + j\omega L_s \\ Z_{22} &= R_s + R_d + 2\alpha R_{ch} + j\omega(L_s + L_d) \end{aligned} \tag{2}$$

where R_{gg} is the gate diode resistance, I_g is the gate current, n is the ideality factor, and α_g ($<1/3$) and α ($<1/2$) are dimensionless factors that fall off with increasing gate current [3]. (High gate currents are crowded at the edge of the gate, avoiding the channel, so the effective channel resistance decreases.) In this regime, the falloff of $\mathrm{Re}\,Z_{11}$ with V_g or I_g is due to the falloff of R_{gg} and that of the other elements is due to the dependence of the α factors on gate current. R_{gg} is connected in parallel with the gate capacitance (Fig. 2(a)). Below the peak, the admittance of the capacitance dominates and above it that of R_{gg}^{-1} dominates. The 2α term in Z_{22} has not been recognized in previous work [4] but is evident in the similarity of the slopes of $2\,\mathrm{Re}\,Z_{12}$ and $\mathrm{Re}\,Z_{22}$ in Fig. 1. We find that the quantities

$$\mathrm{Re}(Z_{22}) - 2\,\mathrm{Re}(Z_{12}) = R_d - R_s \tag{3}$$

are independent of the gate current. If the α term were not present in Z_{22}, this would give $R_d - R_s + (1-2\alpha)R_{ch}$, which is not constant.

In extracting the resistances, there are always more unknowns than equations. R_d can always be obtained from (3) if R_s is known. R_g can likewise be obtained from the difference between $\mathrm{Re}\,Z_{11}$ and $\mathrm{Re}\,Z_{12}$, which is most straightforwardly done at $V_g < 0.6$ V, to avoid the R_{gg} term. This leaves only the equation for $\mathrm{Re}\,Z_{12}$ in two unknowns: R_s and R_{ch}. There are several approaches to this problem. In Fukui's method [5], the sum $R_s + R_d$ is extracted from the gate voltage dependence of $\mathrm{Re}\,Z_{22}$, using a model of R_{ch} based on a shape of the doping profile that is questionable for ion-implanted MESFET's. The measured end-to-end resistance of a gate stripe could be used to compute the distributed resistance R_g in (1), allowing R_s and R_{ch} to be obtained from the equations for Z_{11} and Z_{12}. But since this resistance usually cannot be measured on the same structure as the device under test, unless the gate resistance uniformity is very good, large errors in R_s and R_{ch} can result. Finally, a method we have used for some HEMT's is to bias the FET's at as high a gate voltage as possible and assume that $\mathrm{Re}\,Z_{12} = R_s$. The last method works best for short-gate-length FET's where R_{ch} is small; hence the amount R_s is overestimated is minimal.

The method we have adopted is to extract R_{ch} and R_s from the gate-current dependence of $\mathrm{Re}\,Z_{12}$, as proposed by Mahon *et al.* [6]. We measure the S parameters at three or more gate voltages (usually 0.8, 1, and 1.2 V for GaAs MESFET's) and obtain the average values of $\mathrm{Re}\,Z_{12}$. To solve (2), we initially guess at a value of R_{ch}, calculate the α's from the measured gate current I_g and R_{ch} using formulas discussed below, subtract αR_{ch} from $\mathrm{Re}(Z_{12})$, and iterate R_{ch} until we find zero slope in the dependence of R_s on V_g or I_g. The ideality factor can be measured at smaller gate voltages or can be solved iteratively by first subtracting the $\alpha_g R_{ch}$ term from $\mathrm{Re}\,Z_{11}$ and finding the ideality factor from the change in the remaining part of $\mathrm{Re}\,Z_{11}$ with kT/I_g [4].

The key to this method relies on the accuracy of α and α_g, which have been computed by Lee *et al.* [3] for the dc end-resistance method. However, in dc end-resistance measurements, either the source or drain electrodes are floating, and all the gate current is collected on the other electrode. S-parameter measurements are done at zero drain voltage, and the gate current is partitioned between the drain and source electrodes. The boundary conditions of the two problems are different; hence Lee's values cannot automatically be adopted.

We modeled the α's as a 2-port problem, using SuperCOMPACT [7]. The gate was modeled as a series of 20 parallel capacitors $(C_{gs} + C_{gd})/20$ and resistors $(20R_{gg})$ connected to a chain of resistors such that the sum channel resistance is 1 Ω (Fig. 2(a)). We then varied R_{gg}, and computed the real parts of the Z matrix. As R_{ch} is 1 Ω and $R_s = R_d = R_g$ were assumed to be 0, at low frequency $\mathrm{Re}\,Z_{12}$ is equal to α in (2) and $\mathrm{Re}\,Z_{11} - R_{gg}$ is α_g. The results are shown in Fig. 3, where, as in Lee's

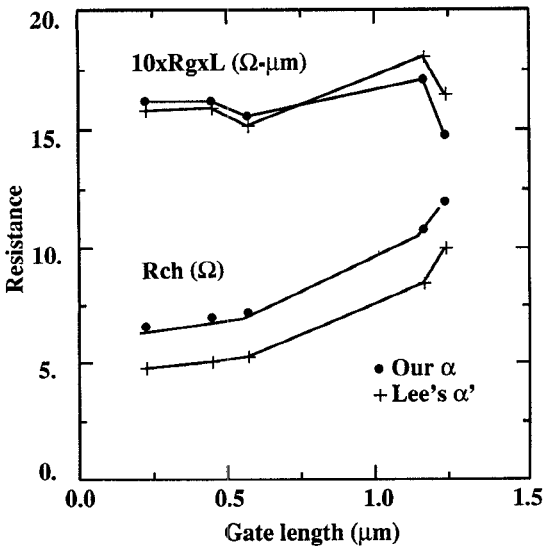

Fig. 4. The product of the extracted R_g and the gate length multiplied by 10 and the extracted R_{ch} values using our α's and those of Lee *et al.* [3] for different measured metal gate lengths.

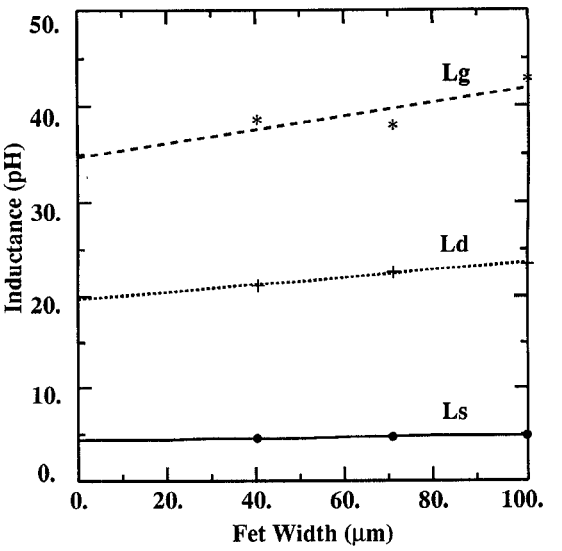

Fig. 5. Inductances versus gate width.

paper $i = R_{ch} I_g / nkT = R_{ch} / R_{gg}$. As expected, α_g goes to 1/3 and α goes to 1/2 at small i. Our α is close to Lee's α (but not their α'), and our α_g approaches α at large i. At large i, the FET can be viewed as a gate with nearly no resistance connecting two small resistors on each end whose values are αR_{ch} (Fig. 2(b)). There is essentially no current in the channel in that case; the channel is shorted by the gate metal. The Z matrix at large i is given by

$$\mathrm{Re}(Z_{11}) = \mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = \alpha R_{ch}$$
$$\mathrm{Re}(Z_{22}) = 2\alpha R_{ch} \tag{4}$$

which shows that α_g must approach α at large I_g. To compute the α's in the extraction procedure, we used analytical formulas similar to those derived by Lee *et al.* [3].

As a test of this method we examined data for different gate lengths L where we expected that R_g would vary as $1/L$ and R_{ch} as L. We found that the product $R_g L$ is indeed nearly constant and is not very dependent on whether our α's or those of Lee *et al.* are used in the extraction (Fig. 4). The R_{ch}'s differ. When Lee's α' replaces α in (2), smaller channel and larger source resistances are needed to fit $\mathrm{Re}\, Z_{12}(I_g)$ because α' falls off more steeply with i. R_{ch}/L is not constant though. We believe this is physical and occurs because, inside the narrower channels, surface depletion regions encroach on both sides of the gate; this reduces the electron concentration under the gate and, because of the high fields, reduces the mobilities.

III. Inductance Extraction and Results

Above $V_g = 0.6$ V, the inductances are extracted by dividing the imaginary parts of the three Z matrix elements by ω (Eq. (2)). The resulting inductances fluctuate from frequency point to point as a consequence of S-parameter precision. Averaging over frequency improves the precision of the extracted inductances somewhat. Below $V_g = 0.6$ V, the capacitance term usually dominates the term in $L_s + L_g$ in (1), and even by a careful least-squares fitting of $\mathrm{Im}\, Z_{11}$ to a function of ω, the resulting gate inductances are usually inaccurate. Although it appears from (1) that L_s and L_d can be straightforwardly extracted at all biases, (1) is actually an approximation which breaks down when R_{ch} becomes large. Starting with the intrinsic Y matrix for $V_{ds} = 0$ (and for pedagogical purposes neglecting C_{ds}), Z_{12} can be shown to be

$$Z_{12} \sim R_s + \frac{R_{ch}}{2}\left[1 - \frac{j\omega C R_{ch}}{4}\right] + j\omega L_s. \tag{5}$$

The imaginary part of Z_{12} really gives a term proportional to $L_s - CR_{ch}^2/8$, where $C = C_{gs} + C_{gd}$. For a typical 0.25×100 μm^2 low-noise FET at $V_g = -1$ V, R_{ch} is 69 Ω and $C = 50$ fF, giving a -30 pH contribution to the imaginary part of Z_{12}. The actual L_s is 4 pH, so if L_s were extracted from (1), the apparent source inductance would be negative.

Fig. 5 shows inductances extracted at $V_g = 1.2$ V for 0.25 μm low-noise MESFET's versus the gate width. The near independence of gate width suggests that most of the observed inductance comes from the pad metal, and not the gate fingers themselves. The expected value of the gate inductance for the active FET can be determined from an equation similar to that for obtaining the distributed gate resistance R_g:

$$L_g = \rho_{lg} W / 3n^2 \tag{6}$$

where ρ_{lg} is the gate inductance per unit gate width W, and n is the number of fingers. The value of ρ_{lg} depends on the mutual inductance with the source and drain fingers and the self-inductance; we expect for ρ_{lg} some value between that appropriate for isolated microstrips [8, eq. (3-52)] and that for coplanar waveguides [8, eq. (3-73)]. Those formulas give 16 pH and 4 pH respectively for 0.25×100 μm^2 FET's, which are small compared with the extracted $L_g = 42$ pH. The observed slope in L_g is 7 pH per 100 μm width, which is within range of these two formulas, indicating that less than 20% of L_g comes from the active-FET region. With multifingered FET's, the active-FET inductances fall off as n^{-2}, but the added metal needed to connect all of the fingers may increase the net inductances.

In conclusion, even if the active-FET inductances are bias dependent (as suggested in [9]), the values principally come from elements extrinsic to the active FET region.

TABLE I
SENSITIVITY OF EXTRACTED INTRINSIC-FET ECP'S TO THE COLD-FET ECP'S (%/%)

ECP:	g_m, C_{gs}	C_{gd}	C_{ds}	R_{ds}	τ	R_i
Linear regime: $V_g = 0$, $V_{ds} = 0.2$ V						
R_s	0.49	−0.45	1.81	−0.46	···	−2.35
R_d	0.61	0.61	2.35	−0.57	···	−0.75
R_g			−0.07		···	−7.32
L_s			1.17		···	−0.16
L_d			3.46		···	0.52
Saturated current $V_g = 0$, $V_{ds} = 2$ V						
R_s	0.15	−0.16	0.20	−0.15	−0.19	−0.98
R_d	0.03	0.03	0.07		−0.31	−0.05
R_g			0.05		0.09	−2.22
L_s						−0.36
L_d					−0.11	0.16
Pinched-FET: $V_g = -2$, $V_{ds} = 2$ V						
R_s	0.01				−0.07	−0.61
R_d				0.11	−0.11	−0.48
R_g					0.11	2.49
L_s						−0.03
L_d						0.06

Absolute values smaller than 0.02 are usually omitted. The sensitivity of L_g is always smaller than 0.02.

IV. COLD-FET PARAMETER EFFECTS ON EXTRACTED INTRINSIC-FET ECP'S

The essential assumption of the cold-FET method is that the values of the resistances and inductances obtained at $V_g > 0.8$ V, $V_{ds} = 0$ are the same at other gate and drain biases. While this is certainly true of R_g and the approximation is good enough for the inductances, R_s may be gate-bias dependent because of the lateral extension of the gate depletion region at low gate voltages [10], and R_d must be drain-bias dependent for $V_{ds} > 1$ V. At high V_{ds}, part of the drain-channel dipole in GaAs MESFET's resides in the region normally part of R_d, and the electron velocities there are saturated [10]. The question considered in this section is how sensitive are the intrinsic ECP's to these possible bias dependences? A large sensitivity would affect the physical interpretation of the intrinsic-FET ECP's.

Sensitivity matrices are one way of examining this question. These are computed by fitting intrinsic ECP's using the method of [2] or [6] with the extracted cold-FET parameters. Then each cold-FET parameter is changed by 10%, the ECP's are refitted, and the difference between each initial and refitted ECP is computed. Table I gives the sensitivities for a 0.22×100 μm^2 low-noise MESFET biased in the linear, saturated-current, and pinched-FET regimes. The extraction method is analogous to the method used to convert extrinsic dc values of g_m and R_{ds} (subscript e) to intrinsic values (subscript i) [11]:

$$P_{mi} = \frac{P_{me}}{1 - R_s g_{me} - (R_d + R_s)/R_{dse}}$$

$$R_{dsi} = R_{dse} - R_s - R_d - g_{me} R_s R_{dse} \tag{7}$$

where $P = g_m$ or C_{gs}. In the linear regime C_{gs} is approximately equal to C_{gd} and the sensitivity is the same as for g_m (except the sign is reversed for C_{gd}). All three are sensitive to the values of both R_s and R_d, through the term in $(R_d + R_s)/R_{dse}$. However, in the saturated-current and pinched-FET regimes, R_{dse} is much greater than R_s and R_d; thus g_m, C_{gd}, and C_{gd} are only sensitive to the term in $g_{me}R_s$. Likewise, R_{ds} is directly sensitive to R_s and R_d in the linear regime. If R_s is made larger, the extracted intrinsic R_{ds} is smaller, because in the extraction process R_s is subtracted from the measured total source–drain resistance. In the saturated-current regime, only R_s affects R_{ds}, through the $g_{me}R_s$ correction.

The sensitivities of C_{ds}, R_i, and τ are more complicated. In the same spirit as (7), analytical relations between the intrinsic and extrinsic values of R_i [12] and C_{ds} can be derived:

$$C_{dsi} = C_{dse}\left[\frac{R_{dsi} + R_d + R_d}{R_{dsi}}\right]^2 + \frac{L_s + L_d}{R_{dsi}^2}$$

$$R_{ii} = R_{ie} - R_g - R_s\left(1 - g_m \tau / C_{gs}\right). \tag{8}$$

These show that the intrinsic R_i values are always directly sensitive to the values of R_g and R_s, and in the linear regime where R_{dsi} is small, the intrinsic C_{ds} values are always sensitive to the values of R_s, R_d, L_s, and L_d. The sensitivity of τ is indirect because terms involving C_{gd}, g_m, C_{gs}, and R_i are subtracted from Y_{21} in extracting τ. As g_m is near zero in the linear regime, the sensitivity of the phase factor τ is immaterial.

The change in R_s and R_d with gate bias in the linear regime can be estimated using two-dimensional device simulators [10], [13]. When the gate potential becomes more negative, the lateral extension of the gate depletion region into the source-resistance region increases R_s. This effect was observed by Byun *et al.* [14], but not by Look [15]. Recess etching minimizes this effect, because the high concentration of donors at the edge of the trench minimizes the lateral extension. For our recessed-etched FET, "GATES-2d" calculations [13] using the gate-edge definition of [10] find that R_s is 1% and 20% larger at $V_g = 0$ and $V_g \sim V_{th} = -2$ V than at forward bias. As the sensitivity of the extracted parameters is much smaller at pinchoff, this 20% increase does not affect the accuracy of the extracted ECP's significantly. Tsai and Grotjohn [10] calculated large changes in R_d for unrecessed FET's with $V_{ds} > 1$ V (20% to 400%), but the sensitivity of the extracted ECP's to R_d is small at those biases. Also, recess etching should help to minimize the increase in R_d, because it minimizes the extension of the dipole region into the drain region.

V. CONCLUSIONS

The cold-FET method allows the accurate extraction of FET parasitic resistances and inductances at forward bias. This paper has examined possible bias dependences of these quantities, with attention also given to the sensitivity of the extracted intrinsic-FET ECP's to variations. R_g is independent of the gate and drain biases, and the dependences of the inductances on gate width suggest that most of the observed inductances come from metal extrinsic to the FET fingers, outside of the region affected by bias. For recess etched FET's, R_s increases slowly as the gate bias becomes more negative, but the sensitivity of g_m and the capacitances decreases faster than R_s increases. While we cannot estimate the increase in R_d with drain bias, the sensitivities of the intrinsic ECP's to changes in R_d with bias are small, except for the parameter τ. From the point of view of fitting S parameters, the sensitivity does not matter, as equally good S-parameter fits can be obtained with a range of R_s and R_d values. The problem appears when we try to read physical meaning into the extracted ECP's. This work suggests that the most difficult parameters to interpret physically are C_{ds} in the linear regime and R_i.

ACKNOWLEDGMENT

The first author wishes to acknowledge many useful discussions with J. P. Lanteri and J. Mahon (MA/COM) and with R. Worley (Wright Research and Development Center).

References

[1] W. Curtice and R. L. Camisa, "Self-consistent GaAs FET models," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, p. 1573, Dec. 1984.

[2] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining FET small-signal equivalent circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.

[3] K. Lee, M. Shur, K. W. Lee, T. Vu, P. Roberts, and M. Helix, "Source, drain and gate resistances in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 987–992, June 1985.

[4] R. Vogel, "Application of RF wafer probing to MESFET modeling," *Microwave J.*, vol. 31, pp. 153–162, Nov. 1988.

[5] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell Syst. Tech. J.*, vol. 58, pp. 771–797, 1979.

[6] J. Mahon, C. Weichert, and J.-P. Lanteri, "Unique determination of a scalable FET model," in *Dig. 1989 US Conf. GaAs Manuf. Technol.*, pp. 58–62.

[7] SuperCompact is a trademark of Compact Software Inc., Patterson NJ.

[8] K. C. Gupta, R. Garg, and R. Chadha, *Computer Aided Design of Microwave Circuits*. Norwood, MA: Artech, 1981.

[9] P. H. Ladbrooke, *MMIC Design: GaAs FET's and HEMT's*. Norwood, MA: Artech, 1989, pp. 96–99.

[10] Y. T. Tsai and T. A. Grotjohn, "Source and drain resistance studies of GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 37, pp. 775–781, Mar. 1990.

[11] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 448–450, Feb. 1987.

[12] R. A. Minasian, "Simplified GaAs MESFET model," *Electron. Lett.*, vol. 13, pp. 550–553, 1977.

[13] R. Anholt and S. Swirhun, "Measurement and analysis of GaAs MESFET parasitic capacitances," pp. 1247–1251, this issue.

[14] Y. H. Byun, M. S. Shur, A. Peczalski, and F. L. Schuerrneyer, "Gate voltage dependence of source and drain resistances," *IEEE Trans. Electron Devices*, vol. 35, pp. 1241–1247, Aug. 1988.

[15] D. C. Look, "Schottky barrier profiling techniques in semiconductors," *J. Appl. Phys.*, vol. 57, pp. 377–383, Feb. 1985.

Measurement and Analysis of GaAs MESFET Parasitic Capacitances

R. Anholt and S. Swirhun

Abstract—**From *S*-parameter measurements and subsequent equivalent-circuit parameter extraction for a series of 0.25 μm, ion-implanted GaAs MESFET's with different widths and different gate–source and drain–source spacings, parasitic FET pad capacitances and interelectrode capacitances have been separated from active-FET capacitances. The active-FET fringe capacitances extracted at pinch-off are compared with results from two-dimensional Poisson simulations.**

I. Introduction

It is well known that FET capacitances do not vanish at very negative gate voltages, and FET f_t values do not scale inversely with gate length for constant doping. One reason for these two observations is the presence of parasitic capacitance coming from three components: capacitance on the fringe of the gate in the semiconductor, interelectrode capacitance over the top of the semiconductor, and pad capacitance associated with the measurement. Any measurement technique, be it low-parasitic-on-wafer or bonded-FET *S*-parameter, requires the presence of pads for the probes or bond wires and interconnect metal to the active FET fingers. These elements add parasitic capacitance, which for small-gate-width, small-gate-length FET's can be comparable in magnitude to the active-FET capacitances. Extrapolating measured FET equivalent-circuit parameters (ECP's) for one width and layout to another assuming that the ECP's vary linearly with width in neglect of pad capacitances and inductances is a potential source of error.

Parasitic capacitances are most accurately measured in pinched FET's, where the FET capacitances that scale as the gate length are zero. Two models of the active-FET capacitances have been used. Wasserstrom and McKenna [1] found that the total active-FET fringe capacitance ($C_{gs}+C_{gd}$) is 0.177 pF/mm, independent of the doping, gate length, gate bias, and all other technological parameters. We have examined pinched-FET data from nine different foundries, and always find larger values, in part because of the components from the pad layout, which are not easy to compute. One motivation of the present work is to isolate the three components of parasitic capacitance so that just the active-FET capacitance modeled by Wasserstrom and McKenna can be compared.

The other model of parasitic GaAs FET capacitances is based on electrostatic solutions to Laplace's equation [2]–[5], often obtained in closed form in terms of elliptical integrals [4], [5]. These formulas predict that the interelectrode capacitances depend on the electrode spacing. Formulas such as this were recently applied to computing pinched-FET capacitances for microwave-switching devices [5] where the frequency figure of merit is inversely proportional to the pinched-FET capacitance. In this paper we show such formulas are indeed applicable for undoped GaAs MESFET's, but active-FET capacitances must be computed using techniques similar to those of Wasserstrom and McKenna. We show that even the interelectrode capacitance over the top of the semiconductor cannot be computed with electrostatic formulas; rather it is dominated by the capacitance in the semiconductor.

In this paper we derive a scalable FET model [6]; i.e., capacitances are modeled as $aW+b$, where W is the FET width and a and b are constants. Most circuit modeling programs allow ECP's to be modeled as a linear function of width (aW or $a'W^{-1}$ for resistances) and even allow W to be optimized. However, unless the intercept b is taken into account, varying the width can lead to substantial errors. In particular for our 0.25×100 μm^2 FET's, scaling the pinched-FET C_{gs} to 200 μm without accounting for the intercept leads to a 21% error. Also, it must be realized that the FET embedded in a circuit is coupled by microstrips with their own capacitances that the circuit simulators attempt to compute; hence the constant component that is present in the *S*-parameter measurement is different or absent in the circuit. Not all designs may be sensitive to this fact, but designers should be aware of the presence of the intercept capacitance in scaling FET designs.

II. Fabrication, Measurement, and Analysis Methods

The MESFET's characterized here were fabricated at the Honeywell Systems and Research Center with a conventional

Manuscript received July 16, 1990; revised March 15, 1991. This work was supported by Honeywell and Gateway Modeling through independent research and development grants.

R. Anholt is with Gateway Modeling, Inc., 1604 East River Terrace, Minneapolis, MN 55414.

S. Swirhun is with the Honeywell Systems and Research Center, Bloomington, MN 55420.

IEEE Log Number 9100153.

0018-9480/91/0700-1247$01.00 ©1991 IEEE